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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LIANG, REGINA	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/747,688	PARK, JAE-DEOK	
	Examiner	Art Unit	
	Regina Liang	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/30/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8,10-15,20 and 21* is/are rejected.

7)☒ Claim(s) *3-7,9 and 16-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 2, 10, 11, 13-15, 20, 21 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's admitted prior art (Figs. 1-5, sections [0003]-[0024] of the specification, hereinafter APA).

As to claim 1, Fig. 1 of APA teaches a shift register, comprising a plurality of stages connected cascade for shifting input signals in accordance with a plurality of phase-delayed control signals (C1-C4), a first supply voltage (VSS), and a second supply voltage (VDD), and for applying the shifted input signals as output signals and as input signals of the succeeding ones of stages.

Fig. 3 of APA teaches each of plurality of stages comprising: a first controller (32) for selectively applying an input signal (SP) and a first supply voltage (VSS) to a first node (Q) arranged between first to third transistors (T1-T3) that form a conductive path between a supply line of the input signal (SP) and an input line of the first supply voltage (VSS); a second controller (34) for selectively applying the first supply voltage (VSS) and the second supply voltage (VDD) to a second node (QB) arranged between fourth and fifth transistors (T4, T5) forming a conductive path between an input line of the second supply voltage (VDD) and the input line of the first supply voltage (VSS); and an output buffer (36) for selectively applying a predetermined control signal (C1) and the

first supply voltage (VSS) as an output signal (SO1) to a stage output line between sixth and seventh transistors (T6, T7) forming a conductive path between the input line of the first supply voltage (VSS) and an input line of the predetermined control signal (C1).

Fig. 2 of APA teaches when the fourth transistor (T4) is turned off and when the fifth transistor (T5) is turned on, the fifth transistor (T5) sustains a voltage present at the second node (QB) equal to the first supply voltage (VSS) if the fourth transistor is turned off (in Fig. 2, during the first period of time, t1, the SP turns the T5 on, the VSS is applied to QB node, the T4 is turned off until t4, see [0017], [0020]).

As to claim 2, Fig. 3 of APA teaches the first and second transistors (T1 and T2) include: first and second conductive paths, respectively, arranged between the supply line of the input signal (SP) and the first node (Q); and first and second control electrodes, respectively (the gate of T1, T2), controlling respective ones of the first and second conductive paths in accordance with the input signal (SP) and a first control signal (C4); and the third transistor (T3) includes: a third conductive path arranged between the first node (Q) and the input line of the first supply voltage (VSS); and a third control electrode (gate of T3) controlling the third conductive path in accordance with a voltage present at the second node (QB).

As to claims 10, 11, APA teaches the transistors within each stage have the same channel type or PMOS.

As to claims 13-15, APA teaches the second supply voltage (VDD represents a high state voltage of –8V) is higher than the first supply voltage (VSS represents a low state voltage of 17V; see [0016] of APA).

As to claims 20, 21, APA teaches the shift register connected to a scan driver and a data driver for driving scan lines and data lines of a display device.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 8, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA in view of Yeo et al (US 6,426,743 hereinafter Yeo).

As to claim 8, APA does not disclose the third transistor (T3) includes a dual gate transistor having control electrodes commonly connected to the second node. However, Fig. 6 of Yeo teaches a stage of a shift register comprising a dual gate third transistor (T5, T6) having control electrodes (gates) commonly connected to a node (P2). Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the third transistor (T3) of APA to have a dual gate transistor as taught by Yeo so as to provide "a shift register that is capable of increasing the range of operating voltage as well as presenting a malfunction" (col. 2, lines 49-50 of Yeo).

As to claim 12, Yeo teaches transistors within each stage include NMOS transistors.

Allowable Subject Matter

5. Claims 3-7, 9, 16-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yeo et al (US 6,339,631) and Huq et al (US 5,701,136).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Regina Liang whose telephone number is (571) 272-7693. The examiner can normally be reached on Monday-Friday from 8AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Regina Liang
Primary Examiner
Art Unit 2674

8/30/06